

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-284192  
 (43)Date of publication of application : 29.10.1993

(51)Int.Cl. H04L 29/10  
 G06F 1/12  
 H04B 10/00  
 H04L 7/00

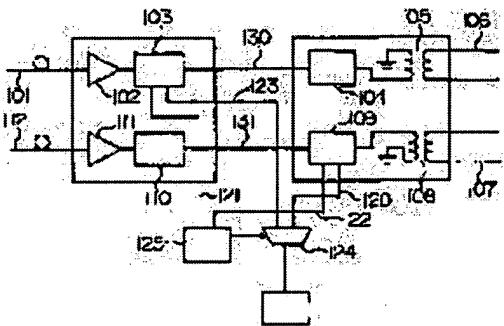
(21)Application number : 04-080118 (71)Applicant : NEC CORP  
 (22)Date of filing : 02.04.1992 (72)Inventor : NAKANE HIDEKI

## (54) CLOCK SYNCHRONIZING SYSTEM

### (57)Abstract:

**PURPOSE:** To decrease the number of types of the equipments forming a network by using a medium converter (light/electricity converter circuit) of a single type.

**CONSTITUTION:** The optical signal received from a receiver optical cable 101 is converted into an electric signal by a light/electricity converter circuit 102 and then sent to an electric interface circuit 104 via a 1st synchronizing signal detecting circuit 103. The signal which undergone the retiming through the circuit 104 is converted into a bipolar signal by a unipolarity/bipolarity converter circuit 105 and sent to a transmitter electric cable 106. Meanwhile the electric signal received from a receiver electric cable 107 is converted into a unipolar signal by a bipolar/unipolarity converting circuit 108 and then sent to an optical interface circuit 110 via a 2nd synchronizing circuit 109. The signal undergone the retiming through the circuit 110 is converted into an optical signal by electricity/light converting circuit 111 of the same type as the circuit 102 and sent to a transmitter optical cable 112.



### LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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**CLAIMS**

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**[Claim(s)]**

[Claim 1] The light / electric conversion circuit which changes into an electrical signal the lightwave signal received from the receiving-side optical cable, The 1st synchronizing signal detector which extracts a clock from a receiving side and extracts m bits from a receiving-side signalling channel while outputting the electrical signal which inputted the electrical signal outputted from light / electric conversion circuit, and was changed and taking the synchronization of a frame, The electrical-and-electric-equipment side interface circuitry which outputs the signal by which inputted the outputted electrical signal and retiming was carried out from the 1st synchronizing signal detector, The unipolar / bipolar conversion circuit which inputs the signal by which retiming was carried out, outputs a bipolar signal, and is sent out to a transmitting-side electrical cable, The bipolar / unipolar conversion circuit which inputs the bipolar signal received from the receiving-side electrical cable, and outputs a unipolar signal, The 2nd synchronizing signal detector which extracts a clock from a receiving side and extracts m bits from a receiving-side signalling channel while outputting the electrical signal which inputted the unipolar signal and was changed and taking the synchronization of a frame, The clock selection circuitry which inputs the clock extracted from the receiving side of the 1st synchronizing signal detector and the 2nd synchronizing signal detector, The control circuit which inputs m bits extracted from the receiving-side signalling channel of the 1st synchronizing signal detector and the 2nd synchronizing signal detector, The clock synchronous system which consisted of a light side interface circuitry which outputs the signal by which inputted the outputted electrical signal and retiming was carried out from the 2nd synchronizing signal detector, and the electrical and electric equipment / optical conversion circuit which inputs the signal by which retiming was carried out, outputs a lightwave signal, and is sent out to a transmitting-side optical cable.

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**DETAILED DESCRIPTION**

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**[Detailed Description of the Invention]****[0001]**

[Industrial Application] About the media-conversion equipment of ISDN, one side is an optical interface, another side is an electric interface, and especially this invention relates to the equipment which has light / electric conversion function in equipment.

**[0002]**

[Description of the Prior Art] Conventionally, that by which what is furnished to a subscriber side with this kind of media-conversion equipment is furnished to a network termination (henceforth "NT") and network side is called the digital circuit access and terminating equipment (henceforth "LT").

[0003] The present condition is that for example, the inside of the exchange or the system in member's house is an electric interface, these equipments have light / electric conversion function, and have the functional almost same function, respectively when the subscriber's loop consists of optical interfaces, but the equipment of dedication is used, respectively when locations within the net differ like whether a subscriber side is furnished or a network side is furnished.

[0004] Moreover, as a basic clock used within these equipments, the clock by the side of a network is used fundamentally. That is, LT will use the clock by the side of an electric interface, and NT will use the clock by the side of an optical interface.

**[0005]**

[Problem(s) to be Solved by the Invention] However, it is expected that the gestalt of a communication network becomes still more complicated as communicative release will be promoted from now on. In this case, as for the media-conversion equipment as for which the synchronization of a clock is made only to one side of the medium which changes like conventional media-conversion equipment, an application is restricted. Specifically, such media-conversion equipment had the trouble that it could use only for the equipment (for example, network termination \*\*\*\*\* NT) which occupies the specific location in a network.

[0006] Moreover, although there was also a method of setting up whether it should synchronize with the clock which prepares a transfer switch into equipment and is received from which medium, when a setup was mistaken, even if it mistook not operating normally and a setup, since it was visible as a slip of a transmission-line interface, there was a trouble that the mistake of a setup could not discover easily.

[0007] the class of device which constitutes a network when one kind of media-conversion equipment (light / electric conversion circuit) is used for the purpose of this invention -- a knife -- it is in \*\*\*\*\*

**[0008]**

[Means for Solving the Problem] The light / electric conversion circuit which changes into an electrical signal the lightwave signal which received this invention from the receiving-side optical cable in order to attain the above-mentioned purpose, The 1st synchronizing signal detector which extracts a clock from a receiving side and extracts m bits from a receiving-side signalling channel while outputting the electrical signal which inputted the electrical signal outputted from light / electric conversion circuit, and was changed and taking the synchronization of a frame, The electrical-and-electric-equipment side

interface circuitry which outputs the signal by which inputted the outputted electrical signal and retiming was carried out from the 1st synchronizing signal detector, The unipolar / bipolar conversion circuit which inputs the signal by which retiming was carried out, outputs a bipolar signal, and is sent out to a transmitting-side electrical cable, The bipolar / unipolar conversion circuit which inputs the bipolar signal received from the receiving-side electrical cable, and outputs a unipolar signal, The 2nd synchronizing signal detector which extracts a clock from a receiving side and extracts m bits from a receiving-side signalling channel while outputting the electrical signal which inputted the unipolar signal and was changed and taking the synchronization of a frame, The clock selection circuitry which inputs the clock extracted from the receiving side of the 1st synchronizing signal detector and the 2nd synchronizing signal detector, The control circuit which inputs m bits extracted from the receiving-side signalling channel of the 1st synchronizing signal detector and the 2nd synchronizing signal detector, It constitutes from a light side interface circuitry which outputs the signal by which inputted the outputted electrical signal and retiming was carried out from the 2nd synchronizing signal detector, and the electrical and electric equipment / optical conversion circuit which inputs the signal by which retiming was carried out, outputs a lightwave signal, and is sent out to a transmitting-side optical cable.

[0009]

[Example] Next, this invention is explained with reference to a drawing.

[0010] Drawing 1 is the block diagram of one example of this invention. In drawing 1, the lightwave signal received from the receiving-side optical cable 101 is changed into an electrical signal by light / electric conversion circuit 102, and is sent to the 1st synchronizing signal detector 103. In the 1st synchronizing signal detector 103, while taking the synchronization of a frame, m bit 121 which similarly extracted the clock 123 extracted from the receiving side from the receiving-side signalling channel to the clock selection circuitry 124 is sent to a control circuit 125. Moreover, the input signal 130 which received and was changed into the electrical signal is sent to the electrical-and-electric-equipment side interface circuitry 104. The signal by which retiming was carried out by the electrical-and-electric-equipment side interface circuitry 104 is changed into a bipolar signal by the unipolar / bipolar conversion circuit 105, and is sent out to the transmitting-side electrical cable 106.

[0011] On the other hand, the electrical signal received from the receiving-side electrical cable 107 is changed into a unipolar signal by the bipolar / unipolar conversion circuit 108, and is sent to the 2nd synchronizing signal detector 109. In the 2nd synchronizing signal detector 109, while taking the synchronization of a frame, m bit 122 which similarly extracted the clock 120 extracted from the receiving side from the receiving-side signalling channel to the clock selection circuitry 124 is sent to a control circuit 125.

[0012] m bits here are explained with reference to drawing 2. Drawing 2 shows the frame format of a primary-PCM-group circuit. F bits of the 4th, the 8th, the 12th, the 16th, the 20th, and the 24th frame are used as a frame alignment signal, and F bits of the 2nd, the 6th, the 10th, the 14th, the 18th, and the 22nd frame are used for detection of a bit error as shown in drawing 2. F bits of odd frames other than the above are m bits said here, and is usable as a data link of 4 kilobits per second. In the one example of this invention, it is considering as the selection information of partner equipment which should synchronize a clock by inserting the specific pattern beforehand decided from the partner equipment which has the clock which should synchronize to these m bits.

[0013] Moreover, the input signal 131 which received and was changed into the electrical signal is sent to the light side interface circuitry 110. The signal by which retiming was carried out by the light side interface circuitry 110 is changed into a lightwave signal by the electrical and electric equipment / optical conversion circuit 111 of the same class as light / electric conversion circuit 102, and is sent out to the transmitting-side optical cable 112.

[0014] In a control circuit 125, it receives from a light side and both electrical-and-electric-equipment side, m bits is checked, and the clock selection circuitry 124 is controlled to choose the receive clock of the way which detected the signal which shows a host side.

[0015]

[Effect of the Invention] As explained above, the effectiveness of making a network design easy with

\*\*\*\*\* is acquired in the class of device which constitutes a network since this invention made the inverter by the side of a network and a subscriber serve a double purpose by one kind of light / electric conversion circuit. Moreover, in order to choose automatically the clock of the side which should synchronize, the effectiveness that malfunction by setting mistake can be prevented is also acquired.

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**DESCRIPTION OF DRAWINGS**

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**[Brief Description of the Drawings]**

[Drawing 1] It is the block diagram of one example of this invention.

[Drawing 2] It is drawing showing the number of multi-framing used for one example of this invention, and the relation of F bits to multi-framing.

**[Description of Notations]**

- 101 Receiving-Side Optical Cable
- 102 Light / Electric Conversion Circuit
- 103 1st Synchronizing Signal Detector
- 104 Electrical-and-Electric-Equipment Side Interface Circuitry
- 105 Unipolar / Bipolar Conversion Circuit
- 106 Transmitting-Side Electrical Cable
- 107 Receiving-Side Electrical Cable
- 108 Bipolar / Unipolar Conversion Circuit
- 109 2nd Synchronizing Signal Detector
- 110 Light Side Interface Circuitry
- 111 Electrical and Electric Equipment / Optical Conversion Circuit
- 112 Transmitting-Side Optical Cable
- 120,123 Clock
- 121,122 m bits
- 124 Clock Selection Circuitry
- 125 Control Circuit

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[Translation done.]

**\* NOTICES \***

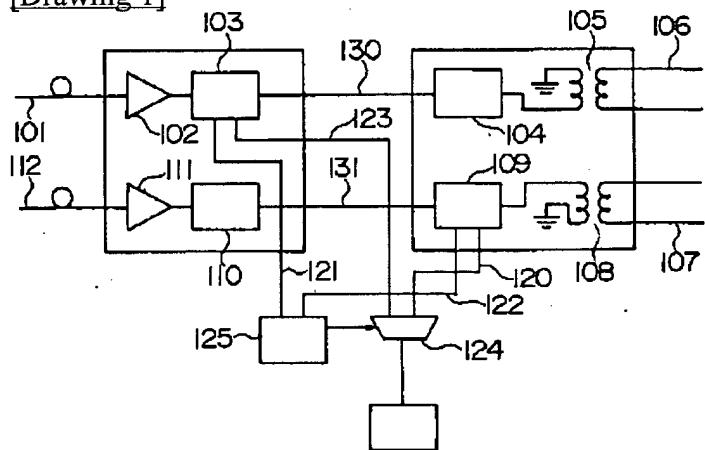
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**DRAWINGS**

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**[Drawing 1]****[Drawing 2]**

マルチフレーム の番号	マルチフレームに おけるFビット	マルチフレームの 番号	マルチフレームに おけるFビット
1	1	13	2317
2	194	14	2510
3	387	15	2703
4	580	16	2896
5	773	17	3089
6	966	18	3282
7	1159	19	3475
8	1352	20	3668
9	1545	21	3861
10	1738	22	4054
11	1931	23	4247
12	2124	24	4440

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[Translation done.]

(19)日本国特許庁 (JP)

(12) 公開特許公報 (A)

(11)特許出願公開番号

特開平5-284192

(43)公開日 平成5年(1993)10月29日

(51)Int.Cl.  
H 04 L 29/10  
G 06 F 1/12  
H 04 B 10/00

識別記号 廣内整理番号

F I

技術表示箇所

8020-5K H 04 L 13/00 309 Z  
7368-5B G 06 F 1/04 340 D

審査請求 未請求 請求項の数1(全4頁) 最終頁に続く

(21)出願番号 特願平4-80118  
(22)出願日 平成4年(1992)4月2日

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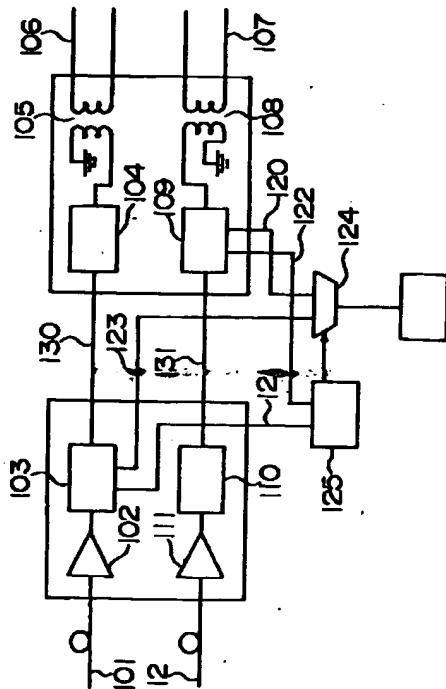
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(54)【発明の名称】 クロック同期方式

(57)【要約】

【目的】 1種類の媒体変換装置(光/電気変換回路)を用いることにより、ネットワークを構成する機器の種類をへらすことにある。

【構成】 受信側光ケーブル101から受けた光信号は光/電気変換回路102で電気信号に変換され、第1同期信号検出回路103を介して、電気側インターフェース回路104に送られる。この回路でリタイミングされた信号は単極性/双極性変換回路105で双極性信号に変換され、送信側電気ケーブル106に送出される。他方、受信側電気ケーブル107から受けた電気信号は双極性/単極性変換回路108で単極性信号に変換され、第2同期信号検出回路109を介して、光側インターフェース回路110に送られる。この回路でリタイミングされた信号は光/電気変換回路102と同一種類の電気/光変換回路111で光信号に変換され、送信側光ケーブル112に送出される。



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## 【特許請求の範囲】

【請求項1】受信側光ケーブルから受けた光信号を電気信号に変換する光／電気変換回路と、光／電気変換回路から出力された電気信号を入力し変換された電気信号を出力しフレームの同期を取ると共に受信側からクロックを抽出し受信側信号路からmビットを抽出する第1同期信号検出回路と、第1同期信号検出回路から出力された電気信号を入力しリタイミングされた信号を出力する電気側インターフェース回路と、リタイミングされた信号を入力し双極性信号を出力して送信側電気ケーブルに送出する単極性／双極性変換回路と、受信側電気ケーブルから受けた双極性信号を入力し単極性信号を出力する双極性／単極性変換回路と、単極性信号を入力し変換された電気信号を出力しフレームの同期を取ると共に受信側からクロックを抽出し受信側信号路からmビットを抽出する第2同期信号検出回路と、第1同期信号検出回路及び第2同期信号検出回路の受信側から抽出されたクロックを入力するクロック選択回路と、第1同期信号検出回路及び第2同期信号検出回路の受信側信号路から抽出されたmビットを入力する制御回路と、第2同期信号検出回路から出力された電気信号を入力しリタイミングされた信号を出力する光側インターフェース回路と、リタイミングされた信号を入力し光信号を出力して送信側光ケーブルに送出する電気／光変換回路とから構成されたクロック同期方式。

## 【発明の詳細な説明】

## 【0001】

【産業上の利用分野】本発明はISDNの媒体変換装置に関し、特に片側が光インターフェース、他方が電気インターフェースで、装置内に光／電気変換機能を有する装置に関する。

## 【0002】

【従来の技術】従来、この種の媒体変換装置で、加入者側に設備されるものは網終端装置（以下、「NT」という。）、ネットワーク側に設備されるものは回線終端装置（以下、「LT」という。）と呼称されている。

【0003】これらの装置は、例えば、交換機内あるいは加入者宅内システムが電気インターフェースで、加入者回線が光インターフェースで構成される場合には、それぞれ、光／電気変換機能を有し、機能的にはほとんど同じ機能を有するが、加入者側に設備されるか、ネットワーク側に設備されるかというように、網内における位置が異なることにより、それぞれ専用の装置が用いられているのが現状である。

【0004】また、これらの装置内で使用する基本クロックとしては、基本的にネットワーク側のクロックが使用される。すなわち、LTは電気インターフェース側のクロックを、NTは光インターフェース側のクロックを使用することになる。

## 【0005】

【発明が解決しようとする課題】しかしながら、今後通信の解放が推し進められるにしたがって、通信網の形態がますます複雑になっていくことが予想される。この場合、従来の媒体変換装置のように、変換を行う媒体の片側だけにしかクロックの同期ができない媒体変換装置は用途が限られてくる。具体的にはこのような媒体変換装置は網の中の特定の位置を占める装置（例えば網終端装置いわゆるNT）にしか使えないという問題点があった。

10 【0006】また、装置の中に切り替えスイッチを設けて、どちらの媒体から受信するクロックに同期するべきかを設定する方法もあるが、設定を間違えると正常に動作しないこと、また、設定を間違えても、伝送路インターフェースのスリップとして見えるために設定の間違いがなかなか発見できないという問題点があった。

【0007】本発明の目的は、1種類の媒体変換装置（光／電気変換回路）を用いることにより、ネットワークを構成する機器の種類をへらすことにある。

## 【0008】

20 【課題を解決するための手段】上記目的を達成するために、本発明は、受信側光ケーブルから受けた光信号を電気信号に変換する光／電気変換回路と、光／電気変換回路から出力された電気信号を入力し変換された電気信号を出力しフレームの同期を取ると共に受信側からクロックを抽出し受信側信号路からmビットを抽出する第1同期信号検出回路と、第1同期信号検出回路から出力された電気信号を入力しリタイミングされた信号を出力する電気側インターフェース回路と、リタイミングされた信号を入力し双極性信号を出力して送信側電気ケーブルに送出する電気／光変換回路とから構成されたクロック同期方式。

30 【0009】  
【実施例】次に、本発明について、図面を参照して説明する。  
【0010】図1は、本発明の一実施例のブロック図である。図1において、受信側光ケーブル101から受けた光信号は、光／電気変換回路102で電気信号へ変換

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され、第1同期信号検出回路103へ送られる。第1同期信号検出回路103では、フレームの同期を取ると共に、受信側から抽出したクロック123をクロック選択回路124へ、同じく受信側信号路から抽出したmビット121を制御回路125へ送る。また、受信して電気信号に変換された受信信号130は、電気側インターフェース回路104へ送られる。電気側インターフェース回路104でリタイミングされた信号は、単極性/双極性変換回路105で双極性信号に変換され、送信側電気ケーブル106に送出される。

【0011】他方、受信側電気ケーブル107から受けた電気信号は、双極性/単極性変換回路108で単極性信号へ変換され、第2同期信号検出回路109へ送られる。第2同期信号検出回路109では、フレームの同期を取ると共に、受信側から抽出したクロック120をクロック選択回路124へ、同じく受信側信号路から抽出したmビット122を制御回路125へ送る。

【0012】ここでいうmビットについて図2を参照して説明しておく。図2はPCM一次群回線のフレーム・フォーマットを示したものである。図2に示されているように、第4、第8、第12、第16、第20、第24フレームのFビットは、フレーム同期信号として使用され、第2、第6、第10、第14、第18、第22フレームのFビットは、ビット誤りの検出のために使用される。上記以外の奇数フレームのFビットが、ここで言うmビットであり、4キロビット/秒のデータリンクとして使用可能である。本発明の一実施例では、このmビットに対して、同期すべきクロックを有している相手装置から予め決められた特定パターンを挿入することにより、クロックを同期させるべき相手装置の選択情報をし

てらすとともにネットワーク設計を容易にするという効果が得られる。また、同期すべき側のクロックを自動的に選択するため、設定ミスによる誤動作を防止できるという効果も得られる。

#### 【図面の簡単な説明】

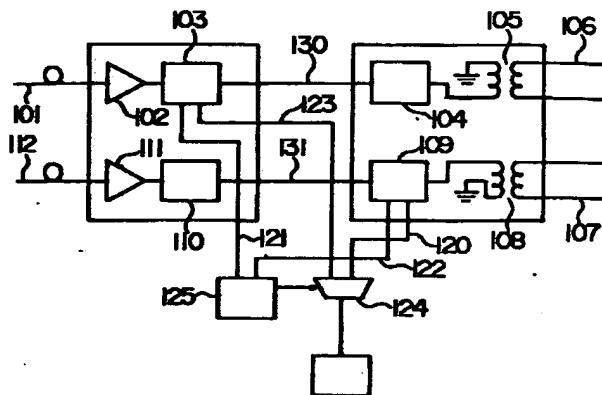
【図1】本発明の一実施例のブロック図である。

【図2】本発明の一実施例に用いるマルチフレームの番号とマルチフレームにおけるFビットの関係を示す図である。

#### 【符号の説明】

- 20 101 受信側光ケーブル
- 102 光/電気変換回路
- 103 第1同期信号検出回路
- 104 電気側インターフェース回路
- 105 単極性/双極性変換回路
- 106 送信側電気ケーブル
- 107 受信側電気ケーブル
- 108 双極性/単極性変換回路
- 109 第2同期信号検出回路
- 110 光側インターフェース回路
- 111 電気/光変換回路
- 112 送信側光ケーブル
- 120, 123 クロック
- 121, 122 mビット
- 124 クロック選択回路
- 125 制御回路

〔四〕



(2)

マルチフレームの番号	マルチフレームにおけるPビット	マルチフレームの番号	マルチフレームにおけるPビット
1	1	13	2317
2	194	14	2510
3	387	15	2703
4	580	16	2896
5	773	17	3089
6	966	18	3282
7	1159	19	3475
8	1352	20	3668
9	1545	21	3861
10	1738	22	4054
11	1931	23	4247
12	2124	24	4440

## フロントページの書き

(51) Int. Q. 5

H04L 7/00

三九四号

厅内整理番号  
Z-7928-5K

E I

技术表示简所

B